University of California, Los Angeles

Department of Electrical and Computer Engineering

EE 215A: Analog Integrated Circuit Design

Fall 2025

Final Project Report

Fully-Differential Folded-Cascode Op-Amp Design

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Due Date: December 8, 2025

1 Introduction

1.1 Project Overview

The primary objective of this project is to design a fully-differential operational amplifier (op-amp) using 180 nm CMOS technology. The design targets high-speed and high-precision performance under a supply voltage of 1.8 V. To satisfy the requirements for high DC gain and wide output swing, a folded-cascode topology is selected as the core amplifier structure.

The project explores the fundamental trade-off between speed and power consumption by implementing two distinct versions of the amplifier:

1.2 Design Specifications

Both designs must adhere to a strict set of performance specifications. The amplifier operates in a closed-loop configuration driving a capacitive load (C_L) of 2 pF. The key design constraints are summarized in Table 1.

Table 1: Design Specifications

Parameter	**Requirement**
Supply Voltage (V_{DD})	1.8 V
Closed-Loop Gain	8
Differential Output Swing	1.6 V_{pp}
Gain Error	$< 1\%$
Load Capacitance (C_L)	2 pF

1.3 System Architecture

The amplifier employs a capacitor-based negative feedback network, as shown in Fig. 1. Ideally, the closed-loop gain is defined by the ratio of the input capacitors (C_1, C_2) to the feedback capacitors (C_3, C_4). Large resistors (R_1, R_2) are placed in parallel with the feedback capacitors to establish a stable DC operating point. These resistors provide a low-frequency feedback path that aligns the input and output common-mode levels, while having negligible effect on the high-speed settling behavior.

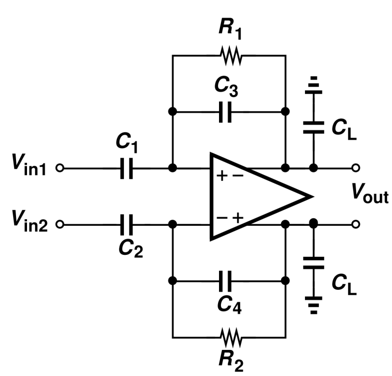

Figure 1: Architecture Overview

2 Design Methodology

2.1 Topology Selection

The folded-cascode topology was selected as the core amplifier structure (Figure 2, left), offering a superior trade-off between output swing and bandwidth compared to telescopic architectures, and better high-frequency performance than two-stage amplifiers. An NMOS input pair was chosen to optimize for speed, leveraging the higher electron mobility (μ_n) to achieve higher transconductance (g_m) and Gain-Bandwidth Product (GBW).

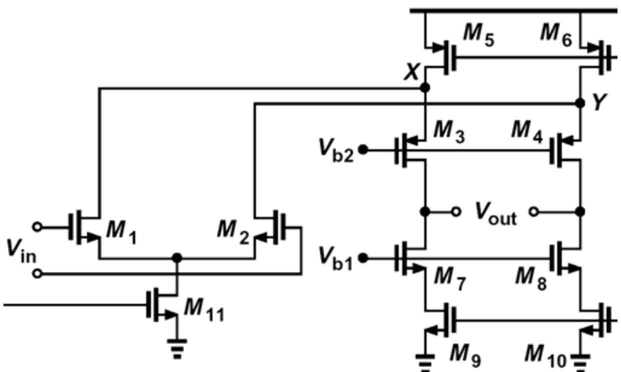

Figure 2: Topology of the fully-differential folded-cascode amplifier.

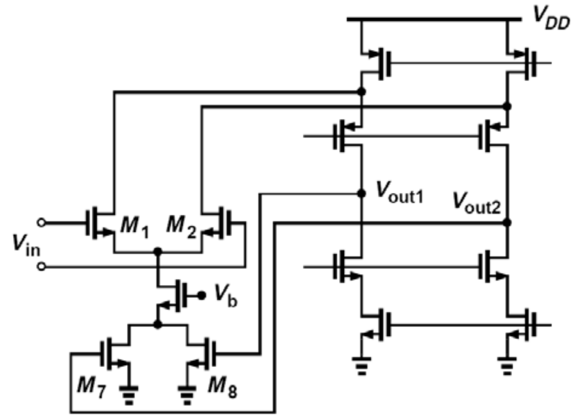

Figure 3: Common-mode feedback (CMFB) using triode-region transistors.

To stabilize the output common-mode voltage ($V_{out,CM}$), a resistive CMFB network utilizing triode-region transistors was implemented (Figure 3). The equivalent resistance is modulated by the output common-mode level according to:

$$R_{out7}||R_{out8} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})_7(V_{out1} + V_{out2} - 2V_{TH})} \quad (1)$$

An increase in $V_{out,CM}$ reduces this resistance, lowering the tail current source gate bias and pulling the output level back. This topology offers three key advantages:

1. Simplicity: Requires minimal active devices, saving area.
2. Swing Preservation: Connects directly to output nodes without consuming voltage headroom, enabling the required 1.6 Vpp swing.
3. Zero Static Power Consumption: Passive sensing network consumes no additional bias current, ideal for Version 2 power constraints.

2.2 Design Parameters and Biasing Strategy

Voltage Headroom and Overdrive Allocation

The design specification requires a differential output swing of 1.6 Vpp. To accommodate this large signal swing under a 1.8 V supply, the overdrive voltages (V_{ov}) were carefully allocated. Each branch needs 0.8v voltage swing range, which means we can assign at most 1v voltage to the Vov for the four transistors' Vov. The basic idea is to assign a larger portion of the voltage to pmos'vov, so the size of pmos transistors will not be too large(creating too much parasitic capacitance).

Capacitor Sizing and Configuration

The closed-loop gain is strictly determined by the ratio of the input capacitor (C_{in}) to the feedback capacitor (C_{fb}). Based on the capacitive feedback topology, the gain relationship is:

$$\left|\frac{V_{out}}{V_{in}}\right| \approx \frac{C_{in}}{C_{fb}} = 8 \implies C_{in} = 8C_{fb} \quad (2)$$

To maximize the feedback factor (β) and slew rate, we adhered to a strategy of minimizing total capacitance. Therefore, C_{fb} was chosen as the minimum value allowed by matching considerations, and C_{in} was scaled accordingly. As specified in the project guidelines, the bottom-plate parasitic capacitance (C_p) is explicitly connected to the source nodes to preserve performance.

Biasing Circuit Implementation

The biasing strategy was designed to ensure robustness and simplicity. For the Common-Mode Feedback (CMFB), the reference voltage (V_{ref}) is generated using a simple resistive voltage divider. For all other transistor biasing, a single ideal current source serves as the master reference, which is mirrored to various branches using diode-connected devices to generate the required gate voltages. Specifically, for the NMOS tail current source of the input pair and the top PMOS current sources, we adopted the structure shown in Figure 4.

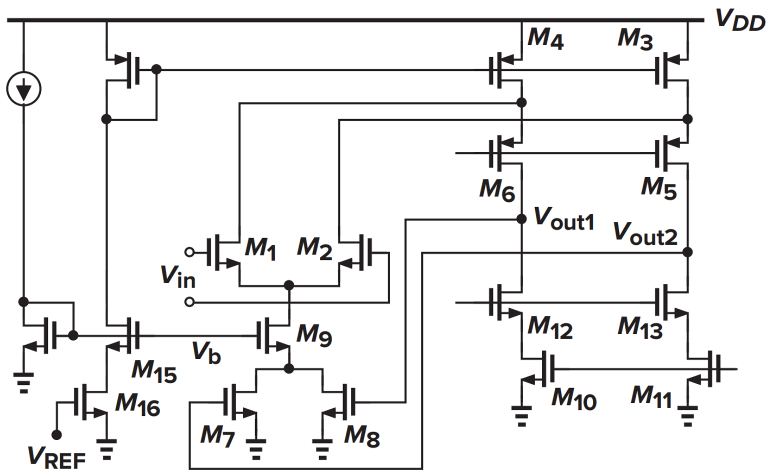

Figure 4: CMFB with Biasing circuit implementation.

To mitigate systematic mismatch caused by Channel Length Modulation (CLM), a resistor is explicitly inserted in the bias branch (e.g., in series with M_{15}). Without this resistor, the drain-source voltage (V_{DS}) of the bias transistor (M_{15}) would not match the V_{DS} of the main tail current source (M_9) in the amplifier core. The added resistor creates a specific voltage drop that equalizes these V_{DS} values, ensuring that the current in the main branch (M_9) accurately tracks the reference current.

Furthermore, to ensure precise current scaling, the bias transistor M_{16} is implemented by splitting it into 2 NMOS devices for matching M7 and M8. To set the current in the main branch to be K times the reference current, the corresponding cascode devices in the main amplifier (M_7, M_8) are sized to be roughly K times the size of the unit devices used for M_{16}. This scaling strategy ensures that the equivalent resistance and operating points are matched, guaranteeing that the gate-source voltage (V_{GS}) of M_9 aligns with that of M_{15} for accurate mirroring.

Analysis of Settling Time

The settling behavior consists of two phases: a large-signal phase and a small-signal phase.

In the large-signal phase, the output is slewing, and the settling time is determined directly by the available current. The slew time T_{slew} is strictly inversely proportional to the tail current I_{tail}, meaning that larger current results in shorter slew duration.

In the small-signal phase, the settling time is determined indirectly by the current. The time constant is approximately proportional to 1/GBW, which can be expressed as

$$\text{GBW} \approx \frac{g_m}{C_{\text{total}}} \approx \frac{g_m}{C_L}.$$

Thus, the small-signal settling time is roughly proportional to C_{total}/g_m, with C_{total} dominated by the load capacitance C_L.

2.3 Some Key Design Principles and Improvements (Common to Both Versions)

Throughout the design process, we explored several techniques to improve the amplifier performance. The most effective strategies are summarized below.

1. **Balancing NMOS and PMOS Output Resistances:** Since the differential output resistance is the parallel combination of the NMOS and PMOS branch resistances, the design ensures that $r_{o,n}$ and $r_{o,p}$ are approximately equal. This prevents one branch from dominating the overall R_{out} and degrading gain.

2. **Increasing the Size of the Middle Cascode Devices:** The two NMOS and two PMOS cascode transistors were scaled up by approximately 1.4×. Because the bias currents remain unchanged, this reduces their overdrive voltages ($V_{ov} = 2I_D/g_m$), thereby increasing g_m and enhancing the effective output resistance R_{out} and overall open-loop gain.

3. **Upsizing the Input Transistors:** The input pair width was increased to boost g_m, improving both the open-loop gain and the unity-gain bandwidth (UGBW), which directly contributes to faster small-signal settling.

4. **Bias Voltage Adjustment for Output Swing:** The bias conditions were tuned so that the top PMOS device and bottom NMOS device operated with V_{DS} close to their respective V_{ov}. This guarantees that all devices remain in saturation while providing sufficient voltage headroom to achieve the required 1.6 V_{pp} differential output swing.

5. **Reducing Input Gate Capacitance:** After completing the main design, the input pair W and L were scaled down proportionally (preserving the W/L ratio) to reduce the input gate capacitance. Simulation confirmed that this resulted in a modest improvement in settling speed.

6. **Reducing CMFB Loading from Large Linear-Region Devices:** After the above optimizations, we initially believed both versions had reached near-optimal performance. However, further inspection of the CMFB structure revealed an additional bottleneck. In this architecture, the output nodes directly drive the gates of two NMOS devices operating in the triode (linear) region. Since our earlier designs used extremely large device dimensions for these transistors, their gate capacitances became excessively high, introducing substantial loading on the output nodes and degrading settling behavior.

   To address this issue, we carefully reduced the device areas by approximately 50% while preserving their aspect ratios to maintain correct resistive behavior in the CMFB network. This significantly decreased the capacitive loading at the output, improving dynamic response without violating any DC gain, saturation, or CMFB stability constraints.

As a result, Version 1's 99% settling time improved from approximately 15 ns to 9.25 ns. Version 2 experienced similar improvement, allowing additional reduction of the tail and bias currents. Ultimately, Version 2's total current was reduced by about 0.4 mA while still meeting all speed and accuracy requirements.

2.4 Version 1 Design (High-Speed, Power-Limited Implementation)

Under the power budget of 10 mW and a supply voltage of 1.8 V, the maximum allowable current is

$$I_{\text{total}} = \frac{10 \text{ mW}}{1.8 \text{ V}} = 5.555 \text{ mA}.$$

The initial goal of the Version 1 design was to first validate the correctness of the amplifier structure and achieve the basic gain and settling specifications. The overall design methodology began with current allocation and overdrive voltage (V_{ov}) selection, followed by device-level sizing through single-transistor simulations.

Initial Device Sizing As a starting point, each cascode branch was conservatively assigned approximately 1.6 mA. Given that Version 1 aims to minimize settling time, the speed is ultimately limited by the available current. Therefore, after completing the preliminary sizing, all MOS devices were scaled proportionally in width so that the total current consumption reached approximately 5.2 mA(excluding bias circuit), maximizing speed while remaining within the power constraint.

For the lower NMOS devices, an overdrive of $V_{ov} \approx 0.2$ V was allocated, yielding a device ratio of roughly $W/L \approx 115$. For the PMOS cascode transistors, the first device used $V_{ov} \approx 0.3$ V and the second $V_{ov} \approx 0.2$ V, resulting in W/L ratios of about 440 and 420, respectively. These choices produced an output common-mode voltage near 0.85 V. Assuming the input common-mode equals the output common-mode, the input pair devices were initialized with $V_{ov} \approx 0.2$ V, resulting in an estimated $W/L \approx 72$.

Using an initial channel length of $L = 0.5$ μm, the simulated open-loop gain reached only approximately 600. Increasing the device lengths to $L_n = 0.8$ μm and $L_p = 1.2$ μm improved the gain significantly. Several iterations of bias refinement and device resizing were performed, leading to the following key design principles that shaped the final Version 1 implementation.

The refinement process described in Section 2.3 ultimately produced a Version 1 amplifier that satisfies the required open-loop gain, output swing, and high-speed settling specifications(**9.25 ns**)under the given power constraint.

2.5 Version 2 Design (Low-Power Design)

Version 2 was designed after completing Version 1, which consumed approximately 5.2 mA of total current and achieved a settling time of about 15 ns (a preliminary, non-final result). Since the settling time is directly determined by the available current—particularly during the large-signal slewing phase—Version 2 initially targeted a reduction of the current to roughly one-third of Version 1 while still maintaining a settling time below 50 ns. This approach enabled the design to meet the time-domain specifications with significantly lower power consumption.

The overall design methodology for Version 2 follows the same principles outlined in Version 1. The NMOS and PMOS channel lengths were again chosen as $L_n = 0.8$ μm and $L_p = 1.2$ μm to maintain sufficient output resistance. A total core current of approximately 1.4 mA was allocated in the initial design, corresponding to roughly 0.7 mA per differential branch.

Overdrive voltages of $V_{ov} = 0.2$ V for the NMOS devices and $V_{ov} = 0.25$ V for the PMOS devices were selected. Individual device dimensions were then determined by sweeping the device widths under fixed-current conditions. This process produced initial device sizes of 40 μm/0.8 μm for the NMOS cascode transistors, 157 μm/1.2 μm for the middle PMOS cascode devices, and 314 μm/1.2 μm for the top PMOS current-source transistors. The NMOS input pair and tail current source were sized as 62 μm/0.8 μm and 80 μm/0.8 μm, respectively.

For the capacitive feedback network, the minimum allowed values were used to maximize the feedback factor and preserve settling performance:

$$C_{fb} = 0.3 \text{ pF}, \qquad C_{in} = 2.4 \text{ pF},$$

maintaining the required closed-loop gain of 8.

As in Version 1, the final design was refined through several iterations. The input transistors and several output-stage devices were slightly upsized to improve transconductance and ensure adequate bandwidth under the reduced current budget. Furthermore, as discussed in Section 2.3, reducing the CMFB loading by shrinking the large linear-region devices significantly improved the settling behavior of both versions. This improvement enabled additional reduction of the bias currents while still satisfying the speed requirement.

As a result, the final Version 2 implementation reduced the main amplifier core current to only **1.08 mA**, achieving the desired balance between power efficiency and settling performance. In DC operation, the measured output common-mode level is approximately 967 mV.

3 Simulation Results

3.1 Schematic of Two Versions of Design

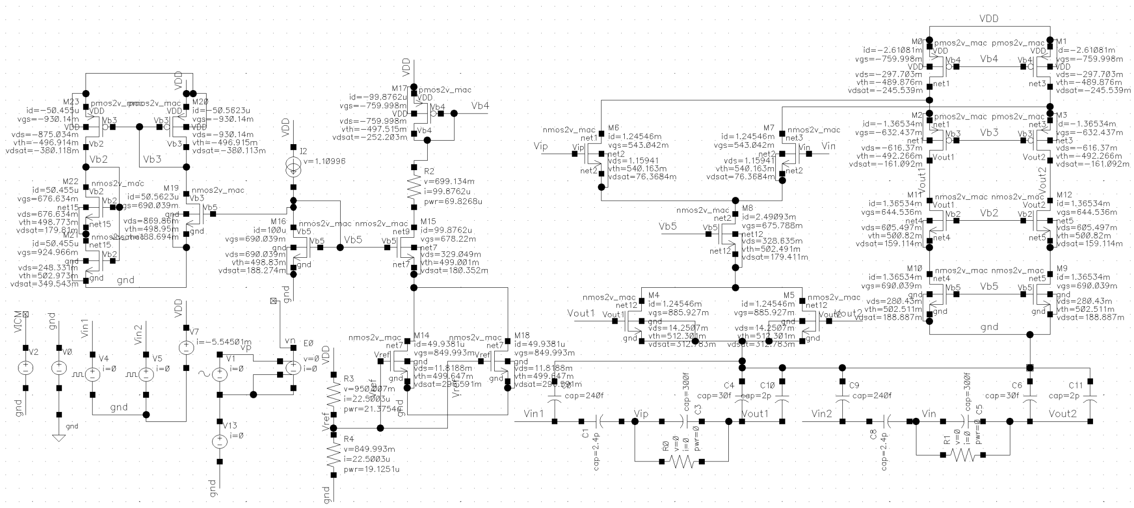

Figure 5: Version 1: Folded-Cascode Amplifier Schematic

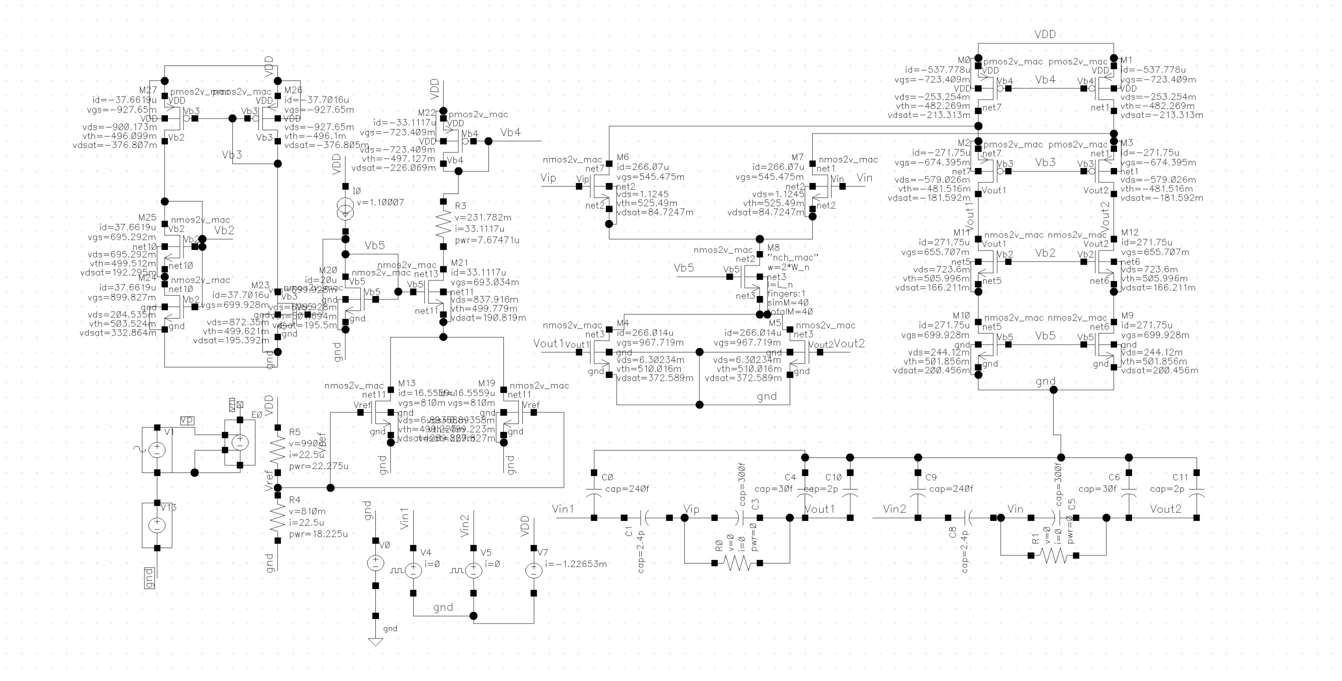

Figure 6: Version 2: Folded-Cascode Amplifier Schematic

V1 Device	V1 (M×W/L)	V1 Total Size	V2 Device	V2 (M×W/L)	V2 Total Size
M6, M7	180×0.96μ/192n	172.8μ/192n	M6, M7	62×0.425μ/192n	26.35μ/192n
M8	185×2μ/800n	370μ/800n	M8	40×1.7μ/800n	68μ/800n
M0, M1	450×2.4μ/1.2μ	1080μ/1.2μ	M0, M1	312×0.85μ/1.2μ	265.2μ/1.2μ
M2, M3	420×3.36μ/1.2μ	1411.2μ/1.2μ	M2, M3	157×0.85μ/1.2μ	133.45μ/1.2μ
M11, M12	92×2.8μ/800n	257.6μ/800n	M11, M12	40×1.19μ/800n	47.6μ/800n
M9, M10	91×2μ/800n	182μ/800n	M9, M10	40×0.85μ/800n	34μ/800n
M4, M5	250×2μ/640n	500μ/640n	M4, M5	240×0.85μ/640n	204μ/640n
M14, M18	1×31.64μ/800n	31.64μ/800n	M13, M19	1×20μ/800n	20μ/800n
M23	1×9.04μ/1.2μ	9.04μ/1.2μ	M27	1×6.8μ/1.2μ	6.8μ/1.2μ
M20	1×9.04μ/1.2μ	9.04μ/1.2μ	M26	1×6.8μ/1.2μ	6.8μ/1.2μ
M17	1×41.45μ/1.2μ	41.45μ/1.2μ	M22	1×17.3μ/1.2μ	17.3μ/1.2μ
M22	1×7μ/800n	7μ/800n	M25	1×4.5μ/800n	4.5μ/800n
M19	1×6.21μ/800n	6.21μ/800n	M23	1×4.3μ/800n	4.3μ/800n
M16	1×12.42μ/800n	12.42μ/800n	M24	1×1.8μ/800n	1.8μ/800n
M15	1×14.2μ/800n	14.2μ/800n	M20, M21	1×4μ/800n	4μ/800n
C1, C8	$C_{in} = 2.4$ pF	2.4 pF	C1, C8	$C_{in} = 2.4$ pF	2.4 pF
C0, C9	$C_{in}/10$	240 fF	C0, C9	$C_{in}/10$	240 fF
C3, C5	$C_{fd} = 0.3$ pF	300 fF	C3, C5	$C_{fd} = 0.3$ pF	300 fF
C4, C6	$C_{fd}/10$	30 fF	C4, C6	$C_{fd}/10$	30 fF
C10, C11	$C_L = 2$ pF	2 pF	C10, C11	$C_L = 2$ pF	2 pF

Table 2: Device and capacitor sizing comparison between Version 1 and Version 2.

3.2 Version 1 Simulation Results

Power Consumption

For Version 1, the total current drawn by the circuit is approximately 5.54501 mA under a 1.8 V supply. This corresponds to a power consumption of

$$P_{\mathrm{V1}} = 1.8 \text{ V} \times 5.54501 \text{ mA} \approx \mathbf{9.98\ mW}.$$

This power level is consistent with the design target for achieving high-speed settling performance.

Open-Loop Gain

As shown in Fig. 7, the open-loop gain of Version 1 reaches approximately **2.485 k**. This gain is well above the minimum required to ensure less than 1% closed-loop gain error, confirming correct operation and sufficient output swing.

During the design process, we observed cases where the simulated open-loop gain was large, yet the closed-loop gain error could not meet the 1% requirement. Further inspection revealed that the issue was caused by insufficient output swing: after a differential input step, the amplifier output did not reach the expected steady-state voltage. By adjusting the bias conditions and slightly refining device dimensions, the output swing was restored and the gain accuracy requirement was satisfied.

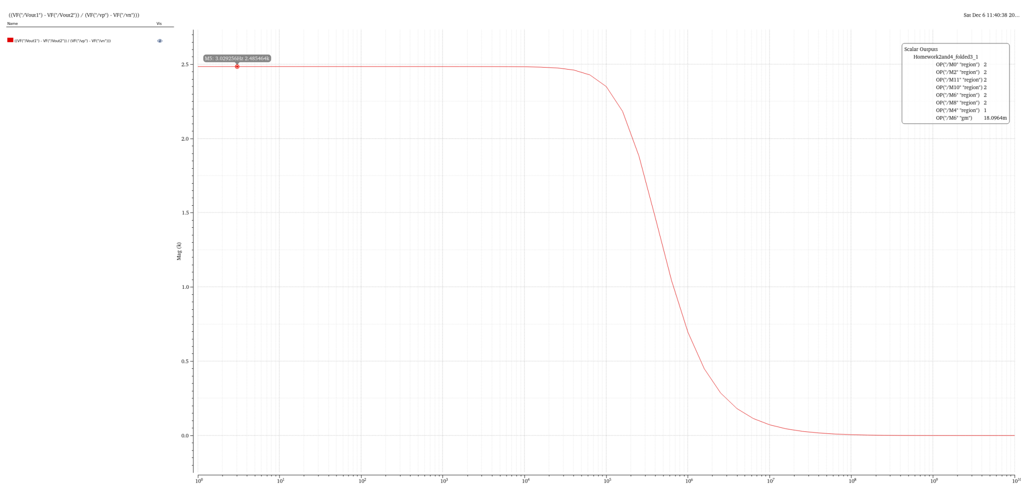

Figure 7: Version 1 open-loop gain.

Settling Behavior

Fig. 8 shows the transient response to a 100 mV differential input step. The output settles to approximately **794.7 mV** (corresponding to the measured steady-state value of about 794.713 mV), exceeding the closed-loop requirement of 0.99×800 mV = 792 mV and therefore satisfying the 1% gain error specification. The 99% settling target corresponding to this steady-state output is

$$0.99 \times 794.7 \text{ mV} \approx 786.75 \text{ mV}.$$

From the waveform, this level is first reached at about **9.25 ns**, which is taken as the 99% settling time. This demonstrates that Version 1 successfully meets the intended high-speed settling requirement.

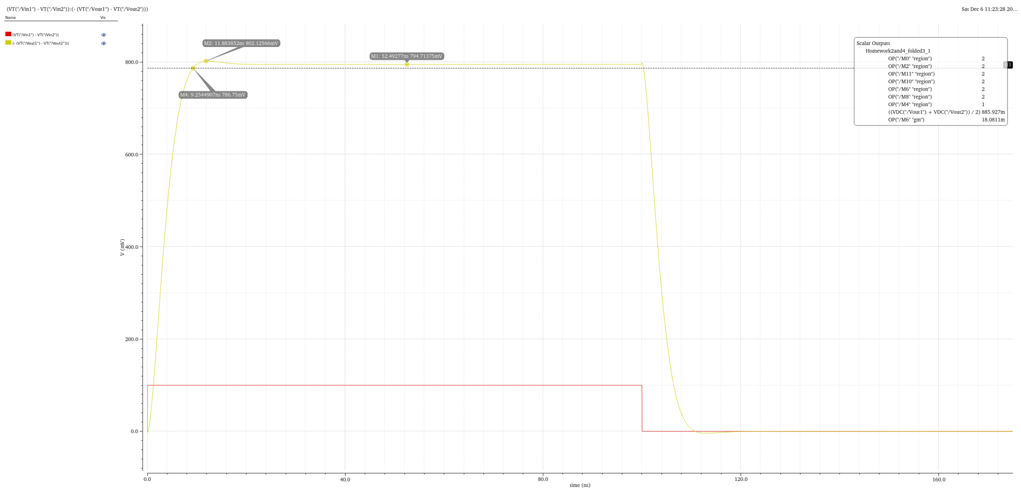

Figure 8: Version 1 transient settling response.

3.3 Version 2 Simulation Results

Power Consumption

For Version 2, the amplifier draws approximately 1.22653 mA from a 1.8 V supply. This corresponds to a total power consumption of

$$P_{\mathrm{V2}} = 1.8\ \mathrm{V} \times 1.22653\ \mathrm{mA} \approx \mathbf{2.21\ mW}.$$

This represents a substantial reduction in power compared to Version 1, consistent with the intended low-power design objective.

Open-Loop Gain

As shown in Fig. 9, the open-loop gain of Version 2 is approximately **1.265 k**. Although lower than Version 1 due to the reduced bias current, this gain remains sufficiently high to satisfy the $< 1\%$ closed-loop gain error requirement.

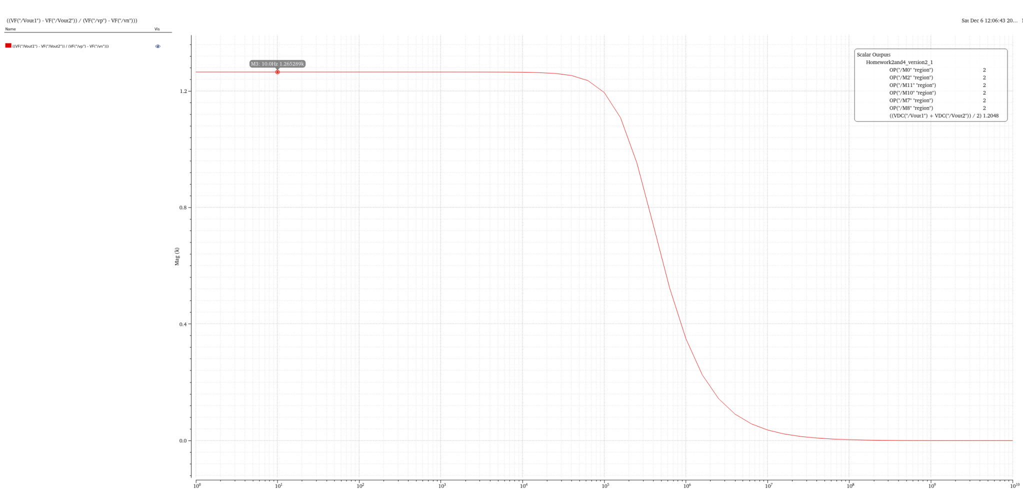

Figure 9: Version 2 open-loop gain.

Settling Behavior

Fig. 10 shows the transient response to a 100 mV differential input step. The differential output settles to approximately **792.61 mV**. The corresponding 99% settling target is

$$0.99 \times 792.61 \text{ mV} \approx 784.68 \text{ mV}.$$

From the waveform, this level is reached at about **45.283 ns**. This improved settling speed, compared to the early Version 2 design, is enabled by the device resizing strategy described in Section 2.3. The reduced device area lowers the load capacitances, improving both slewing and small-signal settling behavior.

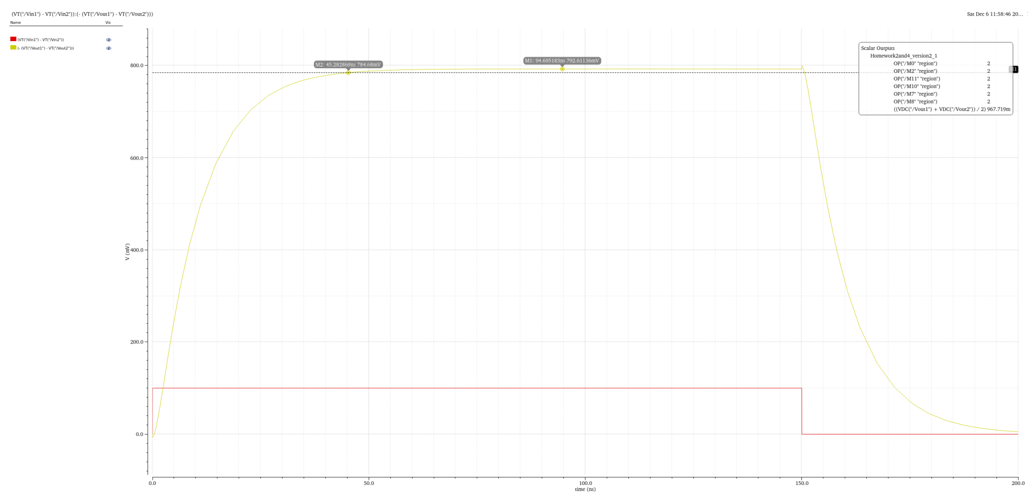

Figure 10: Version 2 transient settling response.

4 Conclusion

In this project, a fully-differential folded-cascode operational amplifier was designed in 180 nm CMOS to meet stringent gain, accuracy, and settling-time requirements under a 1.8 V supply. An NMOS-input folded-cascode architecture, combined with a triode-based resistive CMFB network and capacitive feedback, enabled large output swing, high open-loop gain, and stable common-mode regulation within limited voltage headroom.

Two design versions were implemented to examine the speed–power trade-off. Version 1 draws a total current of approximately 5.545 mA and achieves a 99% settling time of only 9.25 ns, comfortably meeting the gain-error and settling-time constraints. Version 2, after current and sizing optimization, operates at a significantly lower power of about 2.21 mW while still satisfying all DC accuracy and settling requirements.

A key lesson of this project is the central role of current allocation in determining analog performance. Increasing bias current raises device transconductance, improving open-loop gain, bandwidth, and slewing capability so that both large-signal and small-signal components of the response settle faster. Conversely, reducing current lowers power consumption at the cost of slower dynamics. Throughout the optimization process, we intentionally exploited this trade-off to arrive at a low-power Version 2 that remains within specification.

The overall design effort reinforced several core analog principles: systematic current budgeting, careful voltage-headroom allocation, device scaling for gain versus bandwidth, and the necessity of preserving output swing for closed-loop accuracy. The project also deepened our understanding of biasing networks and common-mode feedback (CMFB), both of which are essential for establishing stable operating points and robust differential behavior in modern CMOS analog ICs.