Yanghonghui Chen

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EDUCATION

University of California, Los Angeles — Los Angeles US
Master of Science in Electrical and Computer Engineering – GPA: 3.9/4.0 — Expected Sept. 2025 – Dec. 2026

University of Illinois Urbana-Champaign — Urbana US
Bachelor of Science in Electrical Engineering - GPA: 3.82/4.0 — Sept. 2021 – Jun. 2025

Zhejiang University — Hangzhou China
Bachelor of Engineering in Electrical Engineering - GPA: 3.94/4.0 — Sept.2021 – Jun. 2025

PROJECT EXPERIENCES

High-Precision Fully-Differential Folded-Cascode Op-Amp Design (180nm CMOS)
Course Project (Advisor: Prof. Behzad Razavi) — Oct. 2025 - Dec. 2025
Keywords: *Fully-Differential Folded-Cascode, Triode-Region CMFB, Low-Power Design, Cadence Virtuoso*

- Designed a high-precision, fully-differential folded-cascode op-amp in 180 nm CMOS with NMOS input pairs to maximize gm/BW; implemented a continuous-time CMFB using triode-region devices to preserve headroom and support 1.6 Vpp output swing.
- Engineered a low-power design variant through rigorous power–speed trade-off analysis, achieving 2.21 mW total power (~78% reduction vs. high-speed baseline) while maintaining <1% gain error and 45 ns (99%) settling into a 2 pF load.
- Resolved a critical settling bottleneck by identifying excessive CMFB-network capacitive loading; reduced triode device dimensions by 50% to cut parasitic capacitance—improving large-signal slewing and small-signal settling—and added CLM-compensation resistors in bias branches to ensure VDS-matched current mirrors and robust DC operating points.

Neural Speech Decoding System (Brain-to-Text)
Course Project (Advisor: Prof. Jonathan Kao) — Oct. 2025 - Dec. 2025
Keywords: *PyTorch, LSTM/GRU, BCI, Real-time Decoding, CTC Loss, Google Cloud Platform (GCP)*

- Engineered a real-time, uni-directional LSTM decoder with a specialized non-linear post-stack (Linear-LayerNorm-GELU) to capture long-range temporal dependencies. Enforced strict causal constraints to ensure viability for live Brain-Computer Interface applications, reducing error rates from 23.6% to 19.59%.
- Developed a robust training pipeline using Focal CTC Loss to address severe phoneme class imbalance in intracranial neural data. Stabilized convergence on Google Cloud (Tesla T4) through Gradient Clipping, AdamW optimization, and a sequential learning rate scheduler (Warmup + Cosine Annealing).

High-Speed MASH-1-1-1 Delta-Sigma Modulator Design in 16nm FinFET
Course Project (Advisor: Prof. Hooman Darabi) — Oct. 2025 - Dec. 2025
Keywords: *Verilog, ASIC Design Flow, Logic Synthesis, Static Timing Analysis (STA), Synopsys DC/PrimeTime, TCL, Low Power*

- Engineered a high-speed, pipelined MASH-1-1-1 digital modulator targeting 500 MHz clock frequency. Implemented a robust noise-shaping logic using 5-bit signed arithmetic and bit-extension techniques to handle dynamic ranges (-3 to +4) without overflow, ensuring unconditional stability.
- Synthesized the design using TSMC 16nm FinFET technology with Synopsys Design Compiler. Achieved timing closure across Multi-Mode Multi-Corner (MMMC) conditions (Setup @ SS/125°C, Hold @ FF/-40°C) by developing custom TCL scripts to automatically resolve critical hold-time violations via buffer insertion.
- Conducted gate-level simulations in ModelSim to generate switching activity (VCD) files. Performed high-precision sign-off power analysis using Synopsys PrimeTime PX, achieving a finalized power consumption of 0.178 mW and validating the design against pre-synthesis estimates.

Four-Axis Vacuum Stage for Advanced Nano-Manufacturing
Senior Design (Advisor: Prof. Oleskiy Penkov) — Feb. 2025 - May 2025
Keywords*: STM32, RS-485, Stepper Motor Control, PCB Design, HMI, FSM, C/C++*

- Control System Design: Engineered an STM32-based control system for a 4-DOF robotic arm, using the RS-485 protocol for robust communication with four stepper motor drivers. Developed control logic for precise multi-axis motion and implemented a Finite State Machine (FSM) to automate complex coating sequences.

- Custom PCB Development: Independently designed and validated a custom PCB to integrate the power distribution (24V) and RS-485 communication bus. The design minimized signal interference and voltage drop, ensuring system reliability in a high-vacuum environment.
- HMI & User Interface: Created an intuitive HMI using a TFT touchscreen and physical buttons. The interface provides real-time monitoring of motor status (speed, position) and allows for one-touch execution of preset programs and emergency stops.

Scalable EEG Signal Classification via Federated Learning

Senior Thesis (Advisor: Prof. Howard Yang) Feb. 2025 - May 2025

***Keywords**: TensorFlow, Federated Learning, Personalized FL (pFedMe), EEG, Seizure Prediction*

- Designed and implemented a privacy-preserving pipeline for seizure prediction, processing EEG signals into Pearson Correlation Coefficient (PCC) matrices and training a CNN classifier using four distinct paradigms: Local, Centralized, FedAvg, and pFedMe.
- Demonstrated that standard FedAvg underperforms due to client data heterogeneity and severe class imbalance, while personalized pFedMe significantly improves average sensitivity and F1-scores over FedAvg by adapting to unique patient data.
- Conducted a detailed hyperparameter analysis of the pFedMe personalization weight (λ), revealing that smaller λ values are critical for minority class detection (sensitivity), whereas larger values cause performance to collapse by forcing adherence to a globally biased model.

Optimized Convolutional Layer Implementation Using CUDA

Course Project (Advisor: Prof. Volodymyr Kindratenko) Oct. 2024 - Dec. 2024

***Keywords**: CUDA, Parallel programming, GPU acceleration, Convolutional neural networks (CNNs)*

- Designed and implemented the forward pass of convolutional layers for a modified LeNet-5 architecture using CUDA, optimizing performance for deep learning tasks such as image classification and object detection.
- Implemented a GPU-based forward convolution with a structured Prolog-Kernel-Epilog approach, ensuring memory management, convolution computation, and output transfer, while matching CPU implementation correctness and optimizing performance using Nsight profiling tools.
- Applied advanced GPU programming techniques to optimize the implementation, including streams, GEMM kernels, and kernel fusion, to achieve a target inference time of ≤80ms for 10,000 images from the Fashion MNIST dataset.

RRAM-based Heterogeneous Processing for Multimodal Brain-Computer Interfaces

The University of Hong Kong (Advisor: Dr. Zhengwu Liu) May 2024 - Jul. 2024

***Keywords**: RRAM, Multimodal brain-computer interface, EEG, Compute-in-memory, FDT*

- Simulated representative heterogeneous processing paradigm of P300 signal recognition in Python by using resistive random-access memory (RRAM) with and without fixed parameter disturbance training (FDT).
- Contributed to combining the BCIC IV IIa and the P300 RSVP datasets and designing an RRAM-based multimodal recognizer that integrates components of the pre-trained EEGNet, CSP (Common Spatial Pattern), and a modality-fused classifier to create the multimodal settings.
- Achieved 2.83% higher accuracy using multimodal BCI with FDT than that without FDT and significantly outperformed the MI-alone and P300-alone results by 8.19% and 13.20%, respectively.

Raspberry Pi Based IoT System as a Private Chatbot

Course Project (Advisor: Prof. Deming Chen) Mar. 2024 - May 2024

***Keywords**: IoT System, Raspberry Pi, Machine Learning, Deep Learning*

- Developed an IoT system using Raspberry Pi 4 as a private chatbot with face detection and speaker recognition to guarantee privacy and personal conversations as well as interactions.
- Implemented MTCNN with ResNet and dlib-based face recognition, achieving better performance with the latter; trained the system with one hundred face images for live recognition.
- Built a custom residual neural network with Keras for speaker recognition, achieving 96% accuracy.
- Integrated a server-client architecture using Google Cloud for accelerated processing and implemented speech recognition and TTS for user interaction.

Multiplayer Action Game on FPGA: Crazy Arcade

Course Project (Advisor: Prof. Zuofu Cheng) Mar. 2024 -May 2024

***Keywords**: SystemVerilog, FPGAs, System-on-a-chip, MicroBlaze CPU, VGA*

- Used FPGA for real-time operations, integrating MicroBlaze CPU for game logic and keyboard input processing.
- Developed various modules in SystemVerilog to manage player movements, bomb mechanics, life counts, and game states, interacting through a system bus.
- Incorporated background music by PWM for sound generation, featuring distinct tracks for different game stages.

Cheat-Machine for Game 2048

Course Project (Advisor: Prof. Thomas Moon) Mar. 2024 - May 2024

Keywords*: Embedded DSP, Real-time Signal Processing, Image Processing, Android Studio*

- Developed an app in Android Studio to analyze a live game of 2048, recognizing board digits using image processing.
- Employed efficient template matching for multi-digit recognition, using grayscale conversion, Canny edge detection, and perspective transformation to preprocess images. Used python packages to evaluate the workflow of the application.
- Built an AI engine with an Expecti-max Search algorithm to recommend the optimal move, focusing on corner placement strategies.
- Achieved high accuracy in digit recognition (100% when properly aligned) and consistent AI performance, reaching 1024 tile in 75% of simulations.

Hook&Hair Structure 3D-Printing based on Path Control and 4D Printing Experiment Exploration

Zhejiang University (Advisor: Prof. Guanyun Wang) Jun. 2023 - Aug. 2023

Keywords*: 3D printing, Grasshopper, Rhino, FDM, Path-planning, 4D printing*

- Developed 3D printing techniques for complex hook and hair structures using Rhino and Grasshopper for path planning, generating G-codes for customized printing paths instead of traditional FDM (Fused Deposition Modeling) methods.
- Accomplished applications including hooked ball-mitten toys and hairy objects, requiring precise path control to avoid defects and achieve intricate designs.
- Conducted experiments in 4D printing, modeling deformable planar objects in Fusion360 that transform into stereoscopic shapes when heated.

Over-the-Air-Computation Based Federated Learning Model Establishment & Simulation

Zhejiang University (Advisor: Prof. Howard Yang) Apr. 2022 – Apr. 2023

Keywords*: Edge Computing, Federated Learning, OFDM, Over-the-air Computing, Simulink, Machine Learning, Neural Networks*

- Explored an innovative approach to utilizing private data from distributed databases to train shared models, ensuring user privacy while making use of the data.
- Set up an over-the-air-computation-based communication model in Simulink which could transmit and receive massive data gradients between federated users effectively.
- Combined Machine Learning models like Linear Regression and Deep Learning models like neural networks in MATLAB codes with communication models in Simulink to implement effective edge-computing models.
- Improved the model to adapt to the Large-scale applications by exploiting and modifying existing OFDM Communication Systems.

SKILLS

- **IC Design & EDA Tools:** Cadence Virtuoso, Spectre, Synopsys Design Compiler (DC), PrimeTime (PX for Power Analysis), ModelSim, Virtuoso ADE, 180nm CMOS & 16nm FinFET Technologies, Logic Synthesis, Static Timing Analysis (STA), MMMC Closure, Low Power Design (Clock Gating, Multi-Vth).
- **AI, BCI & Signal Processing:** PyTorch, TensorFlow, Keras, CUDA (Parallel Computing), Federated Learning (pFedMe), Neural Decoding (LSTM/GRU/CTC Loss), EEG Signal Processing, Computer Vision (CNN/ResNet), Google Cloud Platform (GCP).
- **Programming & Scripting:** Python, C/C++, SystemVerilog, Verilog, MATLAB, TCL (EDA Scripting), SQL, Bash, Assembly.
- **Embedded Systems & Hardware:** STM32 (HAL/LL), Raspberry Pi, PCB Design, Finite State Machine (FSM), Communication Protocols (RS-485, UART, SPI, I2C), 3D Printing & Path Planning.