UCLA ECE 215E Final Project: Design of a 5 Gb/s Wireline Transmitter in 180nm CMOS

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1 Introduction

As the demand for high-speed data communication continues to escalate, the design of robust and power-efficient wireline transmitters has become a pivotal challenge in integrated circuit design. This project presents the design and simulation of a complete 5 Gb/s Non-Return-to-Zero (NRZ) transmitter utilizing a standard 180nm CMOS process. The system architecture integrates an 8-to-1 serializer, a high-swing differential line driver, and a low-jitter Phase-Locked Loop (PLL) to provide the necessary multi-phase clocks for data retiming.

1.1 Project Objectives

The primary objective of this design is to synthesize a low-phase-noise, low-spur frequency synthesizer that ensures reliable data transmission at multi-gigabit rates. According to the design specifications, the system must satisfy the following performance metrics:

- **Data Rate:** A minimum NRZ output data rate of 5 Gb/s.
- **Jitter Performance:** The random RMS jitter of the PLL output must be ≤ 4 ps to maintain timing margins.
- **Spur Suppression:** Reference spur amplitudes must be $\leq$ -30 dBc relative to the carrier.
- **Signal Integrity:** A single-ended peak-to-peak output swing of ≥ 0.5 V across a 50 Ω load.

1.2 Division of Labor

Following the recommended system partitioning for the EE 215E final project, the responsibilities were divided as follows:

- **Yanghonghui Chen:** Focused on the Phase-Locked Loop (PLL) system. Key contributions include the design and optimization of the low-noise LC-VCO, charge pump current matching, loop filter stability analysis, and overall loop locking verification.
- **Kaiwen Zhao:** Focused on the Data Chain and Serializer. Key contributions include the logic implementation of the 8-to-1 multiplexer, the optimization of retiming flip-flops for high-speed operation, and the design of the tapered buffer chain to ensure sufficient output eye-opening.

2 Part I: PLL Circuit Design

2.1 System Architecture and Design Philosophy

The core of the transmitter is a Type-II, 3rd-order Phase-Locked Loop (PLL) designed to provide a stable, low-jitter 2.5 GHz clock from a 625 MHz reference signal ($N = 4$). A Type-II architecture is selected for its ability to achieve zero steady-state phase error and its superior tracking performance. The system consists of five primary blocks: a Phase Frequency Detector (PFD), a Charge Pump (CP), a 2nd-order passive Loop Filter (resulting in a 3rd-order system), an LC-tank Voltage-Controlled Oscillator (VCO), and a dual-stage frequency divider.

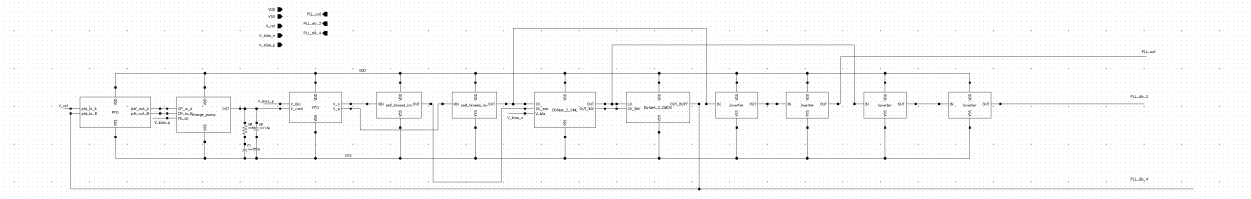
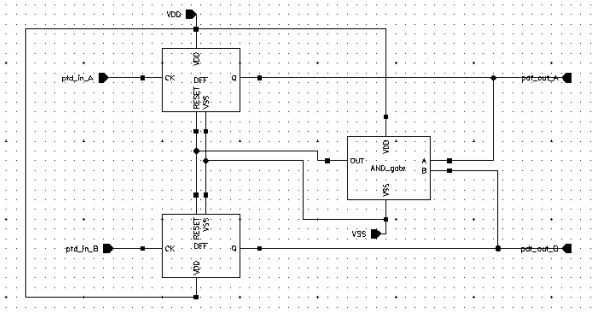


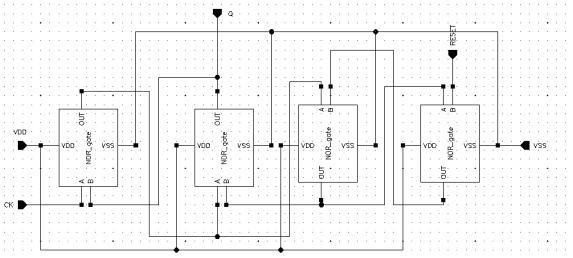
Figure 1: Complete Schematic of PLL in Cadence

2.2 Phase Frequency Detector (PFD)

The Phase Frequency Detector (PFD) is a critical component responsible for comparing the phase and frequency of the 625 MHz reference clock (V_{ref}) and the feedback signal (PLL_div_4). The PFD generates digital error signals, commonly referred to as UP and DOWN pulses, which represent the lead or lag relationship between the two input clocks.



(a) Complete Schematic of PFD in Cadence

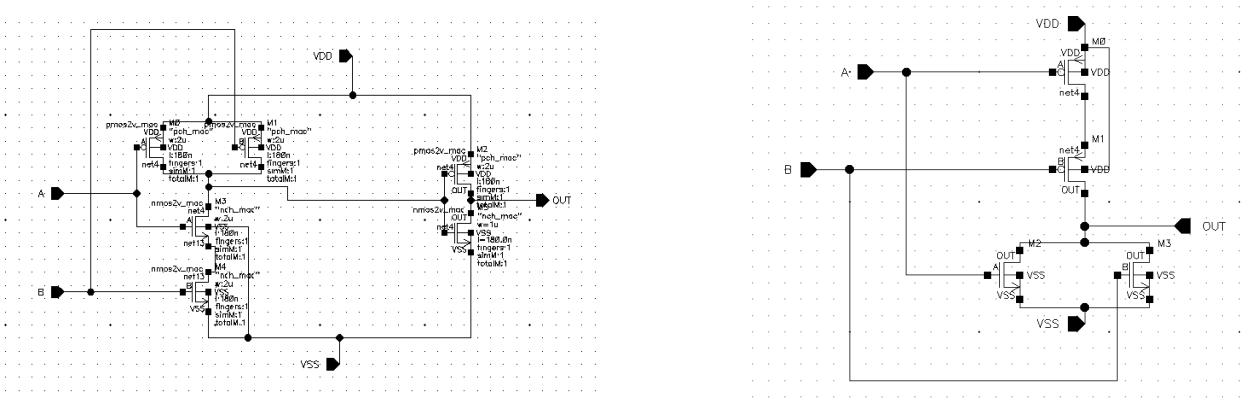


(b) Detailed Schematic of DFF

Figure 2: Architecture of the Phase Frequency Detector and its constituent D-Flip-Flop.

2.2.1 NOR-Gate Based DFF Architecture

In this design, the PFD is implemented using a classic dual D-Flip-Flop (DFF) topology with an asynchronous reset. To optimize for the 180nm process and ensure high-speed operation, each DFF is constructed using a **NOR-latch-based architecture**.



(a) Schematic of AND gate

(b) Schematic of NOR gate

Figure 3: Logic gates used in the PFD implementation.

2.3 Charge Pump (CP)

The Charge Pump (CP) translates digital PFD pulses into an analog current using a current-steering architecture.

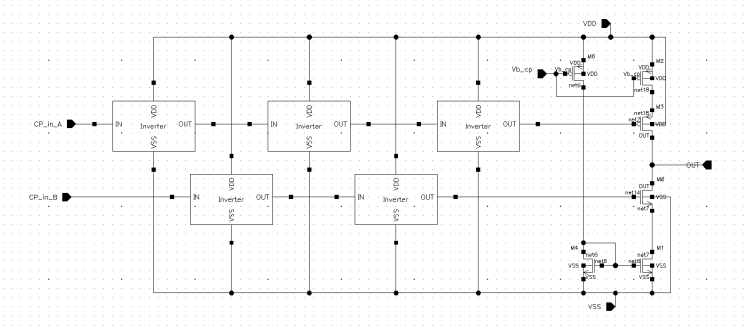


Figure 4: Schematic of the current-steering Charge Pump.

2.3.1 Circuit Implementation

The CP architecture consists of three functional blocks:

- **Bias Generation:** A current mirror network (M_6/M_2 and M_4/M_1) derives stable, symmetrical sourcing and sinking currents from the V_{b_cp} reference, ensuring consistent I_{cp} across the V_{cont} operating range.
- **Switching Network:** Multi-stage inverter chains buffer the PFD pulses (CP_in_A/B) to provide the sharp switching edges and high drive strength necessary for high-speed operation.
- **Current Steering Core:** Switching transistors M_3 and M_0 are placed in series with the current sources to modulate V_{cont} by steering charge directly into or out of the loop filter.

2.4 Loop Filter (LPF)

The loop filter is a critical passive network that defines the dynamics, stability, and noise-filtering characteristics of the Type-II PLL. In this design, a second-order passive low-pass filter is imple-

mented, which, when combined with the $1/s$ characteristic of the VCO, results in a third-order control loop.

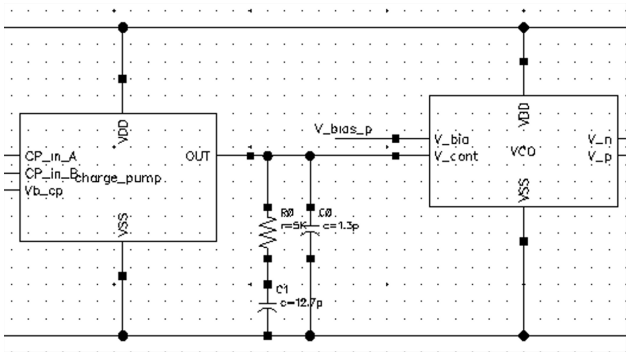


Figure 5: schematic of LPF

2.4.1 Filter Topology and Component Selection

As shown in the schematic (Figure 5), the loop filter consists of a series resistor-capacitor (R_0, C_1) network in parallel with a second capacitor (C_0). The chosen values are:

- **Resistor (R_0):** 5 kΩ
- **Main Capacitor (C_1):** 12.7 pF
- **Ripple Capacitor (C_0):** 1.3 pF

2.5 LC-Voltage Controlled Oscillator (VCO)

The LC-VCO is designed for a center frequency of 2.5 GHz using a cross-coupled NMOS topology with a PMOS tail current source. This architecture is optimized to meet the 4 ps jitter requirement by maximizing the tank quality factor and minimizing transistor noise contributions.

2.5.1 LC Tank Design and Parameter Selection

The resonance frequency is governed by $f_{osc} = 1/(2\pi\sqrt{L_{tot}C_{tot}})$. The parameters were selected as follows:

- **Inductor ($L = 1$ nH):** Two 1 nH inductors ($Q = 8$) are used in a differential configuration. This value was chosen to balance the parallel tank resistance $R_p \approx \omega LQ \approx 125.6\ \Omega$, which directly influences the power-noise trade-off.
- **Capacitance ($C_{tot} \approx 4$ pF):** To achieve 2.5 GHz with $L = 1$ nH, the total capacitance is split between NMOS varactors ($C_{var} \approx 2.61$ pF) and fixed capacitors ($C_{fix} \approx 1.8$ pF). The fixed capacitors stabilize the tank and reduce the K_{vco}, while the varactors provide the necessary tuning range via V_{cont}.

2.5.2 Transistor Sizing and Noise Optimization

The core design involves a critical trade-off between oscillation start-up and phase noise.

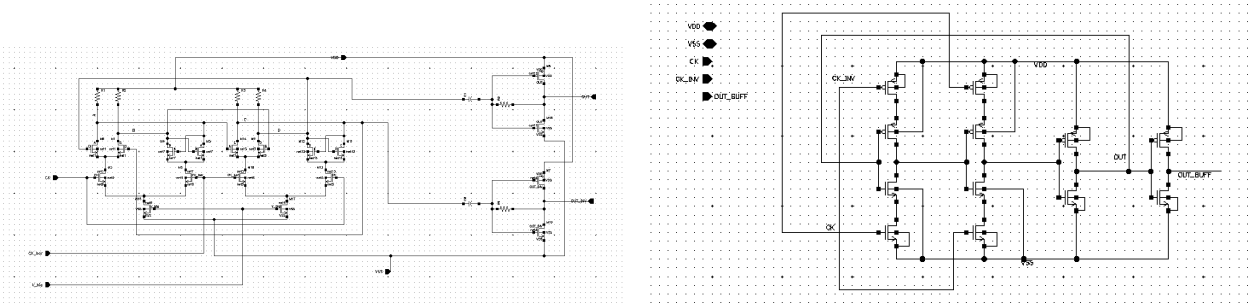
- **Cross-Coupled Pair ($M_1, M_2 = 120\mu$m):** The width was maximized to satisfy two conditions:

    1. **Start-up:** $g_m \geq \alpha/R_p$ (where $\alpha \approx 2-3$ for safety). The large W ensures sufficient negative conductance to overcome tank losses.
    2. **Flicker Noise Mitigation:** Since $S_{i,1/f} \propto 1/(W \cdot L)$, increasing W to 120μm was essential to suppress the 86% flicker noise contribution observed in initial simulations. This optimization achieved a phase noise of -131 dBc/Hz at 10 MHz offset.

- **Tail Current Source ($M_0 = 80\mu$m):** The PMOS source is sized to provide a stable bias current while ensuring sufficient voltage headroom for the LC tank. This maximizes the oscillation amplitude $V_{amp} \approx (4/\pi)I_{tail}R_p$, which improves the phase noise by increasing the signal-to-noise ratio (SNR).

2.6 Frequency Dividers and Level Shifters

The frequency divider chain scales the 2.5 GHz VCO output down to the 625 MHz reference ($N = 4$) using a hybrid CML and C^2MOS architecture to balance speed and power efficiency.



(a) Schematic of CML-based Divide-by-2 stage. (b) Schematic of C^2MOS-based Divide-by-2 stage.

Figure 6: Two-stage frequency divider architecture.

2.6.1 Hybrid Divider Chain

- **CML Stage (2.5 GHz to 1.25 GHz):** A Current-Mode Logic (CML) divider is utilized for the first stage due to its high-speed latch-based topology and low switching noise. The constant current tail source ensures a stable load for the LC-VCO, preventing frequency pulling.

- **C^2MOS Stage (1.25 GHz to 625 MHz):** The second stage employs a C^2MOS divider, which offers lower power consumption and full-swing output at intermediate frequencies. It ensures a 50% duty cycle for the feedback signal, optimizing PFD linearity.

2.6.2 Level Shifting and Swing Restoration

To bridge the low-swing CML output to the CMOS logic levels required by the C^2MOS stage and PFD, a self-biased inverter is implemented.

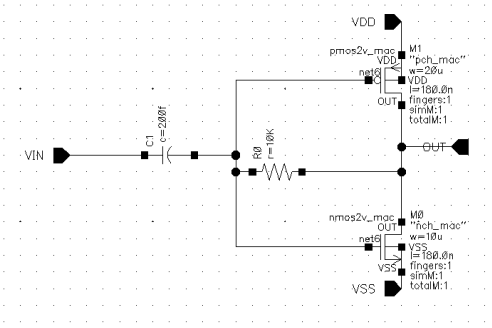


Figure 7: Schematic of the self-biased inverter.

- **Biasing:** A 200 fF capacitor (C_1) provides AC coupling, while a 10 kΩ feedback resistor (R_0) biases the inverter at its switching threshold ($V_{DD}/2$).
- **Restoration:** This configuration restores the signal to a rail-to-rail swing, ensuring reliable triggering of the subsequent CMOS stages.

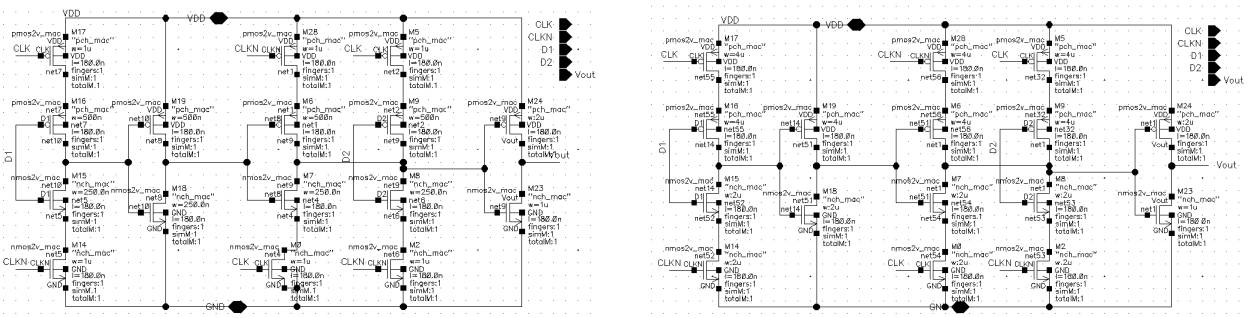
3 Part II: Data Chain Circuit Design

3.1 Serializer (Multiplexer)

The 8-to-1 serializer is implemented as a three-stage 2-to-1 mux tree that converts eight parallel inputs, D_1 to D_8, into a single 5 Gb/s output stream. In the first stage, four C2MOS muxes combine the input pairs (D_1, D_2), (D_3, D_4), (D_5, D_6), and (D_7, D_8), increasing the branch data rate from 625 Mb/s to 1.25 Gb/s. In the second stage, two C2MOS muxes further combine these four intermediate outputs into two 2.5 Gb/s streams. The final stage then uses one C2MOS mux to generate the single serial output. Accordingly, the three clock frequencies provided by the PLL, 625 MHz, 1.25 GHz, and 2.5 GHz, are applied to the three stages respectively so that each stage operates in the correct timing domain as the serialization proceeds.

Each 2-to-1 C2MOS mux selects between two input bits under complementary clock control. When one clock phase is active, one pull-up/pull-down path is enabled and the output follows one input; during the opposite phase, the complementary path is enabled and the output follows the other input. In this way, the mux alternately forwards two data bits onto a single output node, thereby doubling the effective data rate at each stage. Since both PMOS and NMOS networks participate in the selection, the C2MOS structure provides full-swing output while preserving good switching behavior at high speed.

To improve timing alignment, a single C2MOS latch is inserted on one input branch of each mux stage. Based on the design note, the purpose of this latch is to introduce a controlled clock-to-Q delay so that the selected input remains stable during the active selection interval, while transitions occur when that branch is not being selected. This retiming mechanism helps reduce glitches and timing uncertainty at the mux output, which becomes increasingly important at higher operating frequencies. In addition, C2MOS logic is used not only for the latch but also for the mux implementation in all three stages, and the transistor widths are tuned to balance propagation delay, signal quality, and power consumption (Fig. 8).



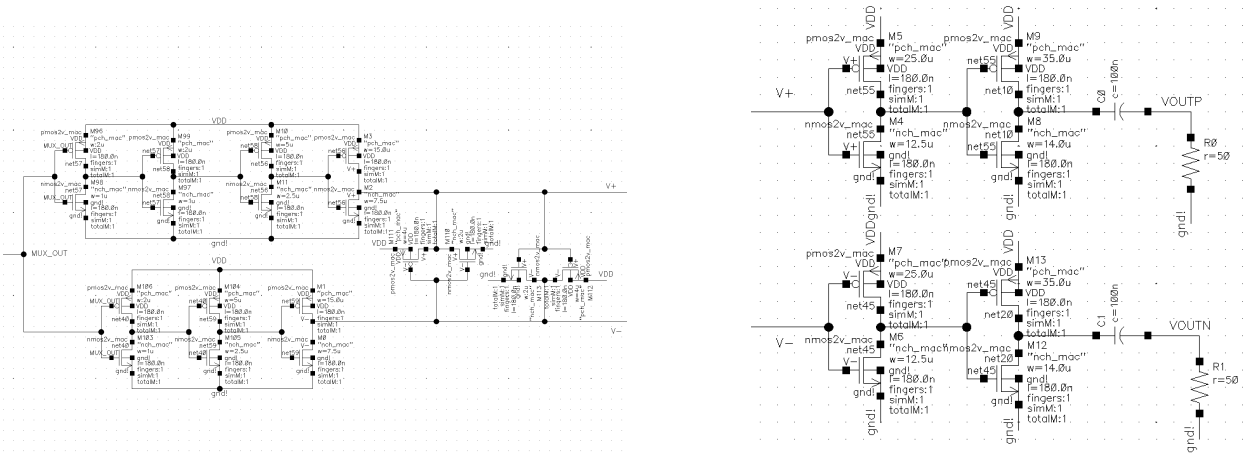
(a) C2MOS muxes for the first and second stages (b) C2MOS muxes for the third stages

Figure 8: C2MOS mux design for all three stages; the topology is identical, with only the transistor widths increased at stage 3 for improved high-speed performance

3.2 Single-Ended to Differential Converter

As shown in Fig. 9(a), the single-ended to differential converter transforms the serializer output MUX_OUT into a differential pair, $V+$ and $V-$, for the following driver stage. It is implemented using two inverter-based branches driven by the same single-ended input at MUX_OUT. The upper branch contains an even number of inversion stages, so $V+$ remains in phase with MUX_OUT, while the lower branch contains an odd number of inversion stages, so $V-$ is inverted. In this way, the circuit generates a differential output pair from a single-ended input.

The converter uses cascaded CMOS inverters with gradually increased transistor widths to achieve both polarity conversion and output buffering. Small input inverters are used to reduce the loading seen by the third-stage mux at MUX_OUT, while larger downstream inverters improve the drive strength for the following load. The PMOS width is chosen to be approximately twice the NMOS width in each stage to obtain more balanced pull-up and pull-down behavior. In addition, a pair of cross-coupled inverters is inserted between the $V+$ and $V-$ nodes to improve output matching and crossing alignment. With similar buffering effort in both branches, the converter reduces delay mismatch and edge-rate imbalance while preserving signal integrity at the differential output. The corresponding eye diagram is shown in Fig. 12(a).



(a) Single-ended to differential converter schematic (b) Differential Line Driver Schematic

Figure 9: Differential converter schematic and its output eye diagram

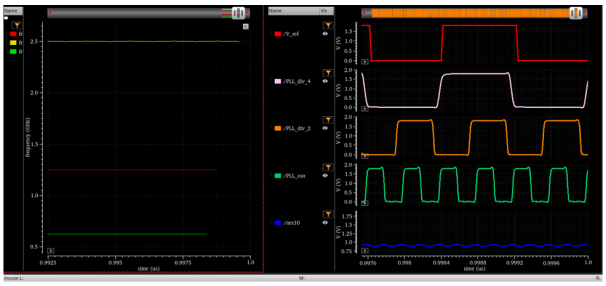
3.3 Differential Line Driver (Pre-driver and Output Stage)

As shown in Fig. 9(b), the final stage is designed as a differential driver that buffers the complementary signals $V+$ and $V-$ and drives the output nodes $VOUTP$ and $VOUTN$. Each branch uses cascaded CMOS inverters, with larger devices in the last stage to provide sufficient drive strength for the output load. At the output, each branch is connected to a 100 nF AC-coupling capacitor followed by a 50 Ω load resistor for transient and eye-diagram evaluation.

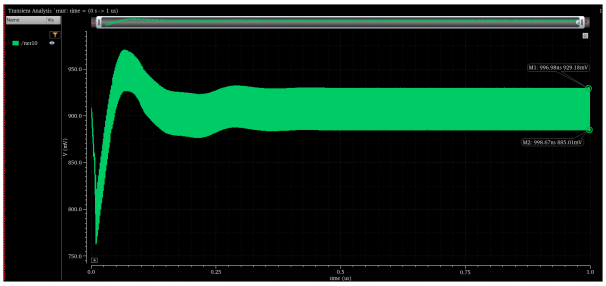
The sizing of the final inverter stage is chosen according to the effective on-resistance of the pull-up and pull-down devices. In the implemented design, the PMOS and NMOS on-resistances are approximately 58.44 Ω and 54.97 Ω, respectively, which fall within the target range of 50 to 75 Ω. This choice provides a compromise between output swing and power consumption. If the resistance is too large, the output swing drops significantly under the load, while if it is too small, the driver becomes excessively strong and consumes more current. Therefore, the selected device sizes provide a balanced trade-off between maintaining sufficient voltage swing and limiting power dissipation.

4 Simulation Results and Analysis

4.1 PLL Locking and Control Voltage



(a) Locked clocks (2.5/1.25/0.625 GHz).

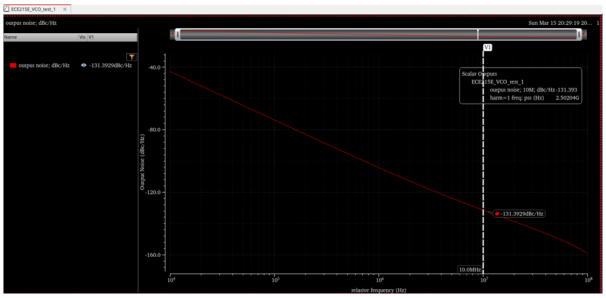


(b) Transient response of V_{cont}.

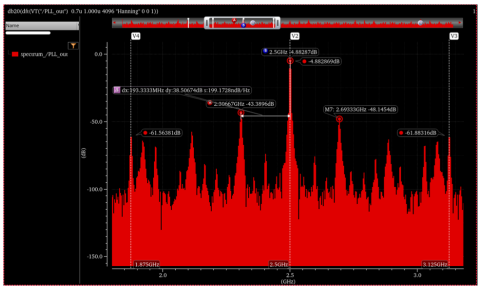
Figure 10: PLL transient simulation demonstrating frequency acquisition and stability.

Transient analysis (Fig. 10) confirms a robust lock at **2.5 GHz**. The control voltage (V_{cont}) settles between **885 mV and 929 mV**; this minimal ripple, achieved via the 3rd-order loop filter, effectively suppresses carrier frequency modulation and ensures low-jitter performance.

4.2 Spectral Performance: Phase Noise and Spurs



(a) VCO Phase Noise (-131.39 dBc/Hz).



(b) FFT Spectrum (-56.82 dBc spur).

Figure 11: Frequency domain analysis showing noise and spectral purity.

The spectral characteristics (Fig. 12) validate the design's high-speed integrity:

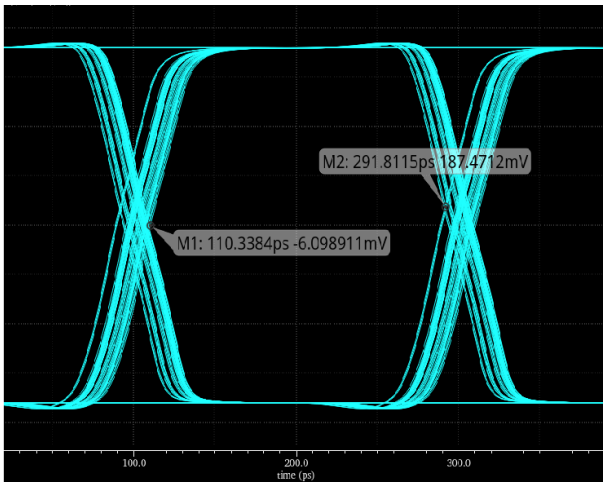
- **Phase Noise**: Measured at **-131.39 dBc/Hz** (10 MHz offset), meeting the **4 ps** integrated jitter target for 5 Gb/s.
- **Reference Spurs**: The primary spur at ±625 MHz offset is **-43.3896 dB**,and the PLL output reference spur amplitude is **-38.5 dB** significantly outperforming the ≤ -30 dBc specification.

4.3 Power Consumption and Efficiency

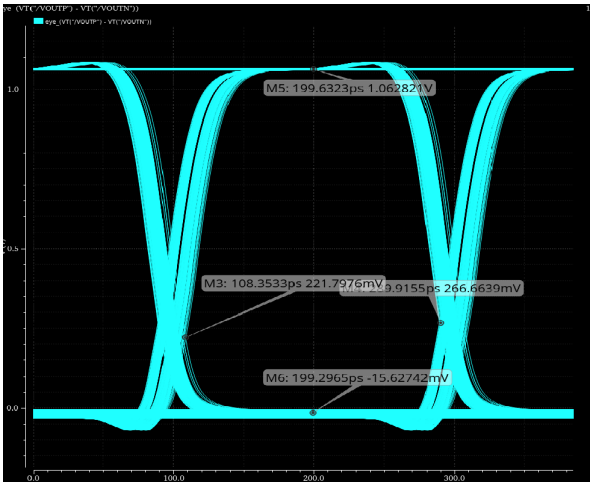
The total power consumption of the complete transmitter—encompassing the PLL, serializer, and differential line driver—is measured at **29.71 mW**. At the target data rate of **5 Gb/s**, the energy efficiency is calculated as:

$$\text{Efficiency} = \frac{P_{total}}{DR} = \frac{29.71 \text{ mW}}{5 \text{ Gb/s}} = 5.942 \text{ pJ/bit} \tag{1}$$

4.4 TX Output Eye Diagram



(a) Eye diagram of the differential output $V+-V-$



(b) Eye diagram of the final output

Figure 12: Frequency domain analysis showing noise and spectral purity.

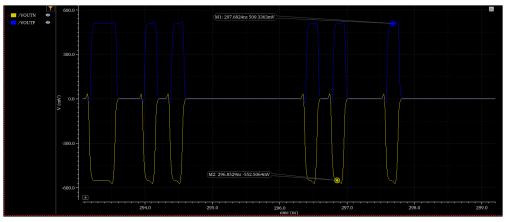


Figure 13: Single-ended output waveform

With random data input generated by 8 independent vpbs, Fig. 12 above compares the eye diagrams at the output of the single-ended to differential converter and at the final output after the differential driver and load. On the left, the eye diagram of $V+-V-$ shows a well-aligned differential signal with a centered crossing point, indicating that the converter generates a balanced complementary pair with good timing symmetry. On the right, after the differential driver, AC-coupling capacitors, and 50 Ω load at each branch, the final output still satisfies the 5 Gb/s target. The measured eye opening is approximately 181.47 ps, which is about 0.9 UI for a 5 Gb/s data rate, and the differential output swing reaches about 1.06 V, while the single-ended output swing is approximately 0.5 V, as shown in Fig. 13. However, compared with the converter output, the final eye is no longer centered at the crossing region and exhibits a more skewed opening. This suggests that the degradation is mainly introduced by the output driver and load network rather than by the converter itself. A likely reason is that, although the nominal output impedance is close to the target value, the final driver still experiences dynamic delay and slew-rate imbalance under the output load, which shifts the eye crossing away from the center.